REMARKS/ARGUMENTS

In view of the foregoing amendments and the following remarks, reconsideration of this application is requested. Claims 1-6 and 9-11 are now pending with claims 1 and 9 being independent. Claim 7 has been canceled. Claims 1 and 9 have been amended. Claims 1 and 9 have been amended to include subject matter corresponding to former dependent claim 7.

Applicant affirms election of Group 1, Claims 1-7 and 9-11 without traverse.

The specification has been amended in response to the Examiner's objection in paragraph 2 of the Office Action to provide the serial numbers of the coassigned applications or patent numbers of issued U.S. patents. The specification has been further amended to correct grammatical errors and minor informalities. No new matter has been introduced.

Claims 1 and 9 have been amended in response to the Examiner's rejections under 35 U.S.C. § 103(a).

As amended, claim 1 describes a method of performing a product operation with rounding in a microprocessor in response to a single rounding multiplication instruction. The method includes fetching a first pair of elements and a second pair of elements. The method also includes forming a most significant product of a first element of the first pair of elements and a most significant element of the second pair of elements and a least significant product of the first element of the first pair of elements and a least significant element of the second pair of elements. The method further includes combining the most significant product with the least significant product to form a combined product, wherein combining comprises shifting the most significant product left by a width of the least significant element of the second pair of elements prior to adding the most significant product to the least significant product. The method also comprises rounding the combined product to form an intermediate result and shifting the intermediate result a selected amount to form a final result.

Amended claim 9 describes a digital system having a microprocessor that can execute a rounding multiplication instruction. The microprocessor includes storage circuitry for holding pairs of elements. A multiply circuit in the microprocessor connects to receive a first number of pairs of elements from the storage circuitry in a first execution phase of the microprocessor responsive to the multiplication instruction, the multiply circuit comprising a plurality of

multipliers. The microprocessor also includes an arithmetic circuit connected to receive a most significant product and a least significant product from the plurality of multipliers. The arithmetic circuit shifts the most significant product by a number of bits prior to adding the most significant product to the least significant product, the arithmetic circuit having a provision for mid-position rounding responsive to the rounding multiplication instruction. The microprocessor comprises a shifter connected to receive an output of the arithmetic circuit, the shifter operable to shift a selected amount in response to the rounding multiplication instructions.

Claims 1-6 and 9-11 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Purcell (5,586,070) in view of either Balkanski et al ((5,253,078) or Saishi et al (6,167,419). Furthermore, the Examiner rejected Claims 1-6 and 9-11 under 35 U.S.C. 103(a) as being unpatentable over Purcell (5,751,622) in view of either Balkanski or Saishi. Moreover, the Examiner rejected Claims 1-6 and 9-11 under 35 U.S.C. 103(a) as being unpatentable over Murakami et al (5,442,799) in view of either Balkanski or Saishi. Applicant requests reconsideration and withdrawal of these rejections for at least the reason that none of the references describes or suggests shifting the most significant product left by a width of the least significant element of the second pair of elements prior to adding the most significant product to the least significant product. The Examiner in his rejections using the prior art cited above does not reject previous claim 7 including the limitations given above because the prior art does not describe or suggest these limitations. Thus, Applicant has combined the limitations of previous claim 7 into independent claims 1 and 9 to overcome the prior art references cited above. For at least these reasons, Applicant respectfully submits that claims 1 and 9 are patentable over the Purcell '070, Balkanski, Saishi, Purcell '622, and Murakami references.

Claims 2-6 and 10-11 depend from independent claims 1 and 9, respectively. Accordingly, Applicant requests reconsideration and withdrawal of the rejections for claims 2-6 and 10-11 for the reasons discussed above with respect to claims 1 and 9.

Independent claims 1-6 and 9-11 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al (6,523,055) in view of either Balkanski or Saishi. However, Yu fails to remedy the failure of Balkanski and Saishi to describe or suggest shifting the most significant product left by a width of the least significant element of the second pair of elements prior to adding the most significant product to the least significant product. Yu also fails to describe or

suggest forming a most significant product of a first element of the first pair of elements and a most significant element of the second pair of elements and a least significant product of the first element of the first pair of elements and a least significant element of the second pair of elements.

Yu, in relevant part, describes in the Abstract and shows in Figures 1A, 1B and 1C multiplying and adding operands A, B, C, D, and E together using a multiplication accumulation circuit and a shifting circuit. Each operand A, B, C, D, and E is stored in an n-bit word with two operands forming 2n-bit double word. In Figure 1B, n-bit word D is multiplied with 2n-bit double word [A,B], D*[A,B] 120A. Similarly, n-bit word C is multiplied with 2n-bit double word [A,B], C*[A,B] 120B. The result of the two multiplications are then shifted and added. In Figure 1C, n-bit word D is multiplied by n-bit word B, D*B 120A, and n-bit word C is multiplied by n-bit word A, C*A 120B. The result of the two multiplications are then shifted and added. Yu does not describe or suggest shifting the most significant product left by a width of the least significant element of the second pair of elements prior to adding the most significant product to the least significant product. In Yu, the multiplication shown in Figure 1C does not produce a most significant product and least significant product as recited and described in Applicant's claim. Yu does not describe or suggest multiplication of D*A (most significant product) and D*B (least significant product) and adding these two products together, D*A+D*B. Also, Yu does not describe or suggest C*A+C*B, A*D+A*C, or B*D+B*C. In Yu, each word in a double word is multiplied by a different word in a second double word and the results added as shown in Figure 1C. For at least these reasons, Applicant respectfully submits that claims 1 and 9 are patentable over Yu, Balkanski, and Saishi.

Claims 2-6 and 10-11 depend from independent claims 1 and 9, respectively. Accordingly, Applicant requests reconsideration and withdrawal of the rejections for claims 2-6 and 10-11 over the Yu, Balkanski, and Saishi references for the reasons discussed above with respect to claims 1 and 9.

In view of these remarks and amendments, Applicant submits that this application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees and/or credit any overpayment to Deposit Account 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,

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Attachments

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